The Graphcore Intelligence Processing Unit (IPU) is a newly developed processor type whose architecture does not rely on the traditional caching hierarchies. Developed to meet the need for more and more data-centric applications, such as machine learning, IPUs combine a dedicated portion of SRAM with each of its numerous cores, resulting in high memory bandwidth at the price of capacity. The proximity of processor cores and memory makes the IPU a promising field of experimentation for algorithms that do not have high arithmetic intensity.
For example, graph algorithms are particularly suitable for these kinds of architectures, since they expose unpredictable, irregular memory accesses that lead to performance losses in traditional processors with pre-caching.

This thesis aims to explore the IPU's suitability and performance of many algorithms across a wide range of algorithms dominates by data movement and memory access.

A partial list may be:

- Fundamental Algorithms (scan, sorting, reductions)
- Graph Algorithms
- Sparse Linear Solvers.